What is claim d is :

1. A method for generating a tracking error signal using differential phase detection, comprising:

reading a plurality of splitting signals, which are inducted by a quadrant photodetector and read by a pick-up, wherein said plurality of splitting signals are further equally divided into two groups signals and at least one signal comprised in each group being mixed;

generating a plurality of up clock signals and a plurality of down clock signals, wherein said plurality of splitting signals and said two groups signals are connected to a plurality of phase detectors, and said plurality of phase detectors generate said up clock signals and said down clock signals;

processing said plurality of up clock signals and said plurality of down clock signals, wherein said up clock signals are processed to obtain a up signal and said down clock signals are processed to obtain a down signal for eliminating phase difference caused by circuit; and

outputting a tracking error signal obtained by comparing said up signal and said down signal.

2. The method according to claim 1, further comprising digitizing said plurality of splitting signals and said two groups signals and then generating said plurality of up signals and said plurality of down signals.

3. The method according to claim 1, wherein a plurality of comparators compare any one of said plurality of splitting signals, said two groups signals and a reference signal one by one, and then input the result to said plurality of phase detectors.

4. The method according to claim 1, wherein any one of said plurality of splitting signals is obtained by processing all of said splitting signals it comprise using adders.

5. The method according to claim 1, further comprising filtering high

frequency noise of said up signal and said down signal, and then output said tracking error signal.

6. The method according to claim 2, wherein said splitting signal A, said splitting signal B and said group signal (A+C) in said digitizing process are input to said plurality of phase detectors through a set of physically-equaled circuit, and said splitting signal C, said splitting signal D and said group signal (B+D) are input to said plurality of phase detectors through another set of physically-equaled circuit.

7. The method according to claim 1, wherein a subtracting circuit is used to process said plurality of up clock signals to obtain said up signal, and said subtracting circuit is used to process said plurality of down clock signals to obtain said down signal.

8. The method according to claim 1, wherein said up signal is corresponded to one of said group signal and said down signal is corresponded to another of said group signal first and said tracking error signal is achieved by comparing said up signal and said down signal.

9. A circuit for generating a tracking error signal using differential phase detection, comprising:

a quadrant photodetector for receiving an optical signal and generating a splitting signal A, a splitting signal B, a splitting signal C and a splitting signal D, wherein said splitting signal A adding said splitting signal C by an adder for forming a group signal (A+C), and said splitting signal B adding said splitting signal D by another adder for forming a group signal (B+D);

a plurality of equalizer for receiving, equalizing and amplifying said splitting signal A, said splitting signal B, said splitting signal C, said splitting signal D, said group signal (A+C) and said group signal (B+D);

a plurality of phase detectors for receiving output of said plurality of equalizers, comparing phase difference between said splitting signal A and said group signal (A+C), said group signal (A+C) and said splitting

signal B, said splitting signal C and said group signal (B+D), and said group signal (B+D) and said splitting signal D, and outputting a plurality of adjusting signals respectively;

a treating circuit for comparing said plurality of adjusting signals outputted by said plurality of phase detectors to obtain an up signal and a down signal;

a plurality of low pass filters for eliminating the high frequency noise of said up signal and down signal; and

a comparator for comparing said up signal and down signal to obtain a tracking error signal.

10. The circuit according to claim 9, said circuit further comprising a plurality of comparators which are connected between said plurality of equalizers and said plurality of phase detectors for transferring signal to digital signal.

11. The circuit according to claim 9, wherein said splitting signal A, said splitting signal B and said group signal (A+C) are inputted through a set of physically-equaled circuit to said phase detector and said splitting signal C, said splitting signal D and said group signal (B+D) are inputted through another set of physically-equaled circuit to said phase detector.

12. The circuit according to claim 9, wherein said plurality of adjusting signals comprises a plurality of up clock signals and a plurality of down clock signals.

13. The circuit according to claim 9, wherein said comparing method of said plurality of adjusting signals are treated by at least one subtractor for eliminating phase difference caused by circuits.

14. A circuit for generating a tracking error signal using differential phase detection comprises:

a first equalizer for receiving a splitting signal A generated by a quadrant photodetector and equalizing and amplifying said splitting

signal A;

a second equalizer for receiving a splitting signal B generated by a quadrant photodetector and equalizing and amplifying said splitting signal B;

a third equalizer for receiving a splitting signal C generated by a quadrant photodetector and equalizing and amplifying said splitting signal C;

a fourth equalizer for receiving a splitting signal D generated by a quadrant photodetector and equalizing and amplifying said splitting signal D;

a fifth equalizer for receiving a group signal (A+C) and equalizing and amplifying said group signal (A+C), wherein said group signal (A+C) is formed by adding said splitting signal A and said splitting signal B by another adder;

a sixth equalizer for receiving a group signal (B+D) and equalizing and amplifying said group signal (B+D), wherein said group signal (B+D) is formed by adding said splitting signal B and said splitting signal D by another adder;

a first phase detector for receiving and comparing said splitting signal A and said group signal (A+C) and outputting an up clock signal and a down clock signal, wherein said splitting signal A being outputted from said first equalizer and said group signal (A+C) being outputted from said fifth equalizer;

a second phase detector for receiving and comparing said splitting signal (A+C) and said group signal B and outputting an up clock signal and a down clock signal, wherein said group signal (A+C) being outputted from said fifth equalizer and said splitting signal B being outputted from said second equalizer;

a third phase detector for receiving and comparing said splitting signal C and said group signal (B+D) and outputting an up clock signal and a down clock signal, wherein said splitting signal C being outputted from said third equalizer and said group signal (B+D) being outputted from said sixth equalizer;

a fourth phase detector for receiving and comparing said group

signal (B+D) and said splitting signal D and outputting an up clock signal and a down clock signal, wherein said group signal (B+D) being outputted from said sixth equalizer and said splitting signal D being outputted from said fourth equalizer;

a treating circuit for processing and comparing said plurality of up clock signals and down clock signals outputted by said plurality of phase detectors to obtain an up signal and a down signal, said up signal being obtained by adding up clock signal outputted by said first phase detector and up clock signal outputted by said second phase detector and then subtracting the result of adding up clock signal of said third phase detector and that of said fourth phase detector, said down signal being obtained by adding down clock signal outputted by said first phase detector and down clock signal outputted by said second phase detector and then subtracting the result of adding down clock signal of said third phase detector and that of said fourth phase detector;;

a first low pass filter for receiving said up signal;

a second low pass filter for receiving said down signal; and

a comparator for comparing output signal of said first low pass filter and said second low pass filter and generating a tracking error signal.

15. The circuit according to claim 14, said circuit for generating said tracking error signal using differential phase detection further comprising:

a first comparator for transferring output signal of said first equalizer to digital signal;

a second comparator for transferring output signal of said second equalizer to digital signal;

a third comparator for transferring output signal of said third equalizer to digital signal;

a fourth comparator for transferring output signal of said fourth equalizer to digital signal;

a fifth comparator for transferring output signal of said fifth equalizer to digital signal; and

a sixth comparator for transferring output signal of said sixth

equalizer to digital signal.

16. The circuit according to claim 14, wherein said splitting signal A, said splitting signal B and said group signal (A+C) are inputted through physically-equaled circuit to said first phase detector and said second phase detector.

17. The circuit according to claim 14, wherein said splitting signal C, said splitting signal D and said group signal (B+D) are inputted through physically-equaled circuit to said third phase detector and said fourth phase detector.

18. The circuit according to claim 14, wherein the same phase offset is caused on the circuit through which said splitting signal A, said splitting signal B and said group signal (A+C) go.

19. The circuit according to claim 14, wherein the same phase offset is caused on the circuit through which said splitting signal C, said splitting signal D and said group signal (B+D) go.

20. The circuit according to claim 14, wherein the comparing of said plurality of up signals and said plurality of down signals are treated by a subtract circuit